CLAIMS

What is claimed is:

1. A method of planarizing a structure on a semiconductor substrate, the method comprising:

providing said semiconductor substrate with raised and lowered regions with substantially vertical and horizontal surfaces, said vertical surfaces having a predetermined height;

depositing filler material over said horizontal surfaces to at least a thickness equal to said predetermined height so as to provide raised and lowered regions of filler material; and

selectively removing said raised regions of said filler material.

2. The method of claim 1, wherein said filler material comprises non-conformal high density plasma oxide.

3. The method of claim 1, wherein adjacent sections of said raised and lowered regions of filler material are separated by at least a gap of exposed underlying material and the selectively removing comprises covering said lowered regions of filler material with a mask and etching said filler material on said raised regions which are not protected by said mask.

4. The method of claim 1, further comprising covering said lowered regions of filler material with a conformal coating, and wherein said selectively removing comprises removing said coating from substantially all of said raised regions, and etching said filler material on said raised regions, wherein during said selectively removing adjacent sections of said upper and lower regions of filler material are separated by at least a gap of exposed underlying material.

5. The method of claim 1, further comprising providing an oxide pad on said semiconductor substrate and providing a nitride pad on said oxide pad, wherein said raised and lowered regions are formed by masking regions of the nitride pad and etching exposed areas of said nitride pad.

6. The method of claim 5, further comprising removing said oxide pad and said nitride pad after selectively removing said raised regions of said filler material.

7. The method of claim 1, wherein the selectively removing comprises selectively etching only said raised regions of said filler material without etching said lowered regions of said filler material.

8. A semiconductor substrate having a planarized trench region formed according to the method of claim 1.

9. A method for planarizing a trench region provided in a semiconductor substrate, the method comprising:

providing the semiconductor substrate with at least one trench region;

applying a filler material in the trench region and on the semiconductor substrate; and

removing only said filler material which is not provided in said trench region.

10. The method of claim 9, wherein said filler material comprises non-conformal high density plasma oxide.

11. The method of claim 9, wherein the removing comprises covering the trench region with a mask and etching said filler material from regions which are not protected by said mask.

12. The method of claim 9, further comprising covering said trench region with a conformal coating, and wherein said removing comprises removing

said coating from substantially all non-trench regions and etching said filler material on the non-trench regions.

13. The method of claim 9, further comprising providing an oxide pad on said semiconductor substrate and providing a nitride pad on said oxide pad, wherein said at least one trench region is formed by masking regions of said nitride pad and etching exposed areas of said nitride pad.

14. The method of claim 9, further comprising removing said oxide pad and said nitride pad after removing the filler material which is not provided in the trench region, wherein adjacent sections of said trench regions and non-trench regions of filler material are separated by at least a gap of exposed underlying material.

15. A semiconductor substrate having a planarized trench region formed according to the method of claim 9.

16. A method of forming a planarized structure on a semiconductor substrate, the method comprising:

providing the semiconductor substrate with a trench region and non-trench regions;

depositing filler material on said trench region and said non-trench regions, said filler material filling said trench region to a predetermined height; and

removing said filler material from said non-trench regions while allowing said filler material in said trench region to remain filled to the predetermined height.

17. The method of claim 16, wherein said filler material comprises non-conformal high density plasma oxide.

18. The method of claim 16, wherein adjacent sections of said trench region and non-trench region of filler material are separated by at least a gap of exposed underlying material and the removing comprises covering said trench regions of filler material with a mask and etching said filler material on said non-trench regions which are not protected by said mask.

19. The method of claim 16, wherein the removing comprises covering said trench regions of filler material with a conformal coating, and wherein said removing comprises removing said coating from substantially all of said non-trench regions, and etching said filler material on said non-trench regions, wherein during the removing adjacent sections of said trench region and non-trench region

of filler material are separated by at least a gap of exposed underlying material.

20. The method of claim 16, further comprising providing an oxide pad on said semiconductor substrate and providing a nitride pad on said oxide pad, wherein said trench region and the non-trench regions are formed by masking regions of said nitride pad and etching exposed areas of said nitride pad.

21. The method of claim 20, further comprising removing said oxide pad and said nitride pad after removing said filler material on the non-trench regions.

22. The method of claim 16, wherein the removing comprises selectively etching said filler material on the non-trench regions without etching said filler material on the trench regions.

23. A semiconductor substrate having a planarized structure formed according to the method of claim 16.